

# User's Manual

SYS8F600VGGA-8265U

Ver 1.0

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# 1. Models and Attentions

## 1.1 Models

This manual is applied to following models:

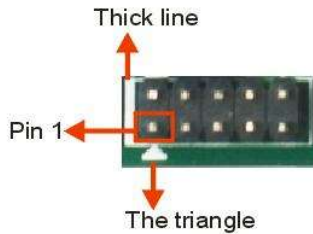
Model	CPU	COM	LAN	USB	HDMI	LVDS /eDP	M.2 Key-B	M.2 Key-M/B	M.2 Key-E	SATA 3.0
8F600-4205U	4205U	6	2	9	2	LVDS	5G/4G	SATA SSD	WIFI+ BT	1
8F600-8145U	i3-8145U	6	2	11	2	LVDS	5G/4G	PCIE/ SATA SSD	WIFI+ BT	1
8F600-8265U	i5-8265U	6	2	11	2	LVDS	5G/4G	PCIE/ SATA SSD	WIFI+ BT	1
8F600-8565U	i7-8565U	6	2	11	2	LVDS	5G/4G	PCIE/ SATA SSD	WIFI+ BT	1

## 1.2 Attentions

1) Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).

2) How to identify the first pin of a header or jumper

- Usually, there is a thick line or a triangle near the header's or jumper's pin 1.



- Square pad, which you can find on the back of the motherboard, is usually used for pin 1.



## 2. Specification

Model		8F600-8565U	8F600-8265U	8F600-8145U	8F600-4205U
CPU	CPU Model	Core™ (Premium-U)			Celeron® (Base-U)
		i7-8565U	i5-8265U	i3-8145U	4205U
	Clock Speed	1.8GHz, up to 4.6GHz	1.6GHz, up to 3.9GHz	2.1GHz, up to 3.9GHz	1.80GHz
	Multi-Core	Quad	Quad	Dual	Dual
	TDP	15W Base, 25W Max			15W
Display <sup>[1]</sup>	1 * LVDS/eDP (Header): LVDS up to 1920x1200@60Hz (default) or eDP up to 3840x2160@60Hz 2 * HDMI (Upright TYPE-A): max resolution up to 4096x2160@30Hz				
Memory <sup>[2]</sup>	Support DDR4-1866/2133/2400 MHz, 1 * non-ECC SO-DIMM Slot, Up to 16GB				
Storage	1 * SATA3.0 7P Connector (with 1 * SATA Power Header) 1 * M.2 (NGFF) Key-M/B Slot (PCIe x4 NVMe/ SATA SSD, 2242/2280) <sup>[3]</sup>				
Ethernet <sup>[4]</sup>	LAN1: 1 * I219 GBE LAN Chip (RJ45, 10/100/1000 Mbps) LAN2: 1 * I211 GBE LAN Chip (RJ45, 10/100/1000 Mbps) (LAN2 colay with R_USB3 on the same position, default support LAN2)				
Audio	Realtek ALC897 Channel HDA Codec, 1 * Front Audio Header (Line-Out + MIC)				
Expansion Slots	1 * M.2 (NGFF) Key-B Slot (3042/3052, PCIE + USB3.0(Premium-U) + USB2.0, support 4G/5G, with 1 * SIM Card Header) <sup>[5]</sup> 1 * M.2 (NGFF) Key-E Slot (PCIE+USB2.0, WIFI+BT, 2230)				
COM	1 * RS232/485 (COM1, Full lanes, DB9/M, RS232/485 SEL by Jumper, PIN1 DCD/5V/12V SEL by res, DCD# default, PIN9 RI/5V SEL by res, RI# default) 2 * RS232 (COM2/3, Full lanes, Header, PIN1 DCD/5V/12V SEL by res, DCD# default, PIN9 RI/5V SEL by res, RI# default) 1 * RS232 (COM4, 7 lanes, Header, PIN1 N/C /5V/12V SEL by res, N/C default, PIN9 N/C /5V SEL by res, N/C default) 1 * RS232 (COM5, 3 lanes, Header, only TX/RX/GND) 1 * RS232/485 (COM6, 3 lanes, Header, only TX/RX/GND)				
USB <sup>[4][5][6]</sup>	4 * USB3.0 (TYPE-A, Rear IO)				
	7* USB2.0 (Header, Internal)			5* USB2.0 (Header, Internal)	
Other Ports	8 * GPIO 1 * System FAN Header 1 * System Reset Header 1 * HDD LED Header 1 * Power LED Header 1 * Power Button Header 1 * CMOS Clear Jumper				
System	Windows 10 64-bit, Linux				
Temperature	Storage: -20~80°C Operating: -10~70°C				
BIOS	AMI UEFI BIOS (Support Watchdog Timer)				

<b>Power Supply</b>	DC 12V 1 * DC 12V Power Input Thread Connector <sup>[7]</sup> 1 * DC 12V Power Input Header
<b>Factor</b>	3.5-inch Standard (146mm * 105mm)

**Notes:**

[1]: Up to three independent displays can be activated at the same time.

[2]: Supported memory frequency is determined by the CPU, supports up to 2400MHz

[3]: Only SATA for Base-U or NVMe/ SATA Auto detected for Premium-U.

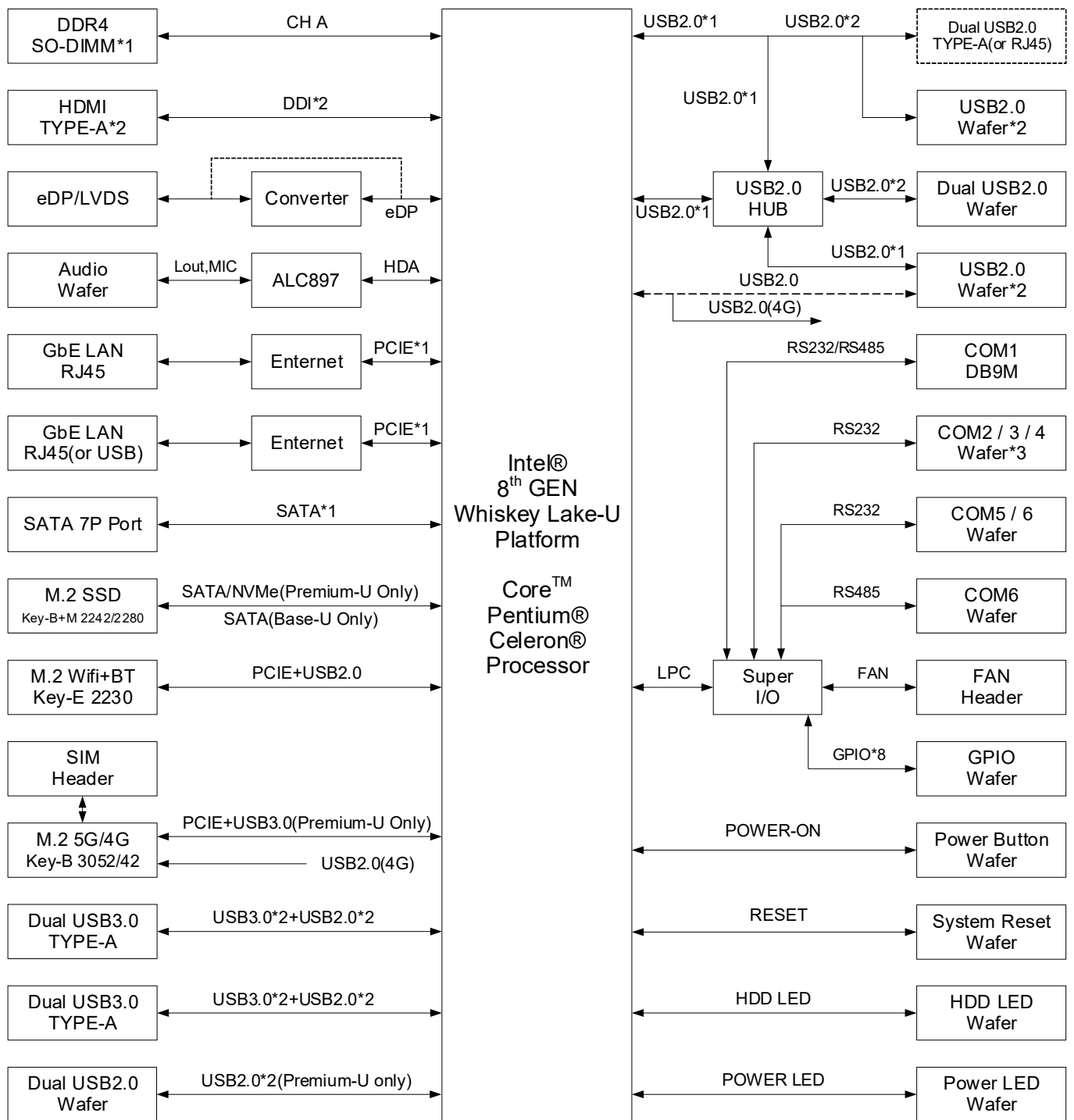
[4]: F\_USB1 and F\_USB2 signal colay with R\_USB3. And LAN2 colay with R\_USB3 on the same position, support LAN2 & F\_USB1/2 by default (R\_USB3 not support).

[5]: USB3.0 of M.2\_B1\_5G1 only support by Premium-U. And USB2\_7 Signal of F\_USB4 colay with M.2\_B1\_5G1, default support M.2\_B1\_5G1. (resistor selectable)

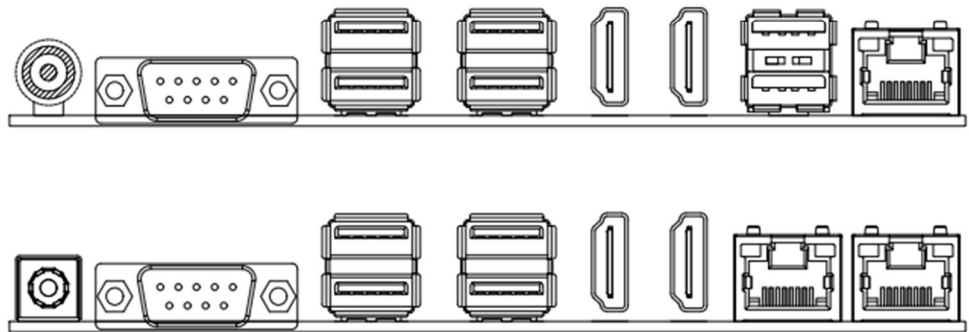
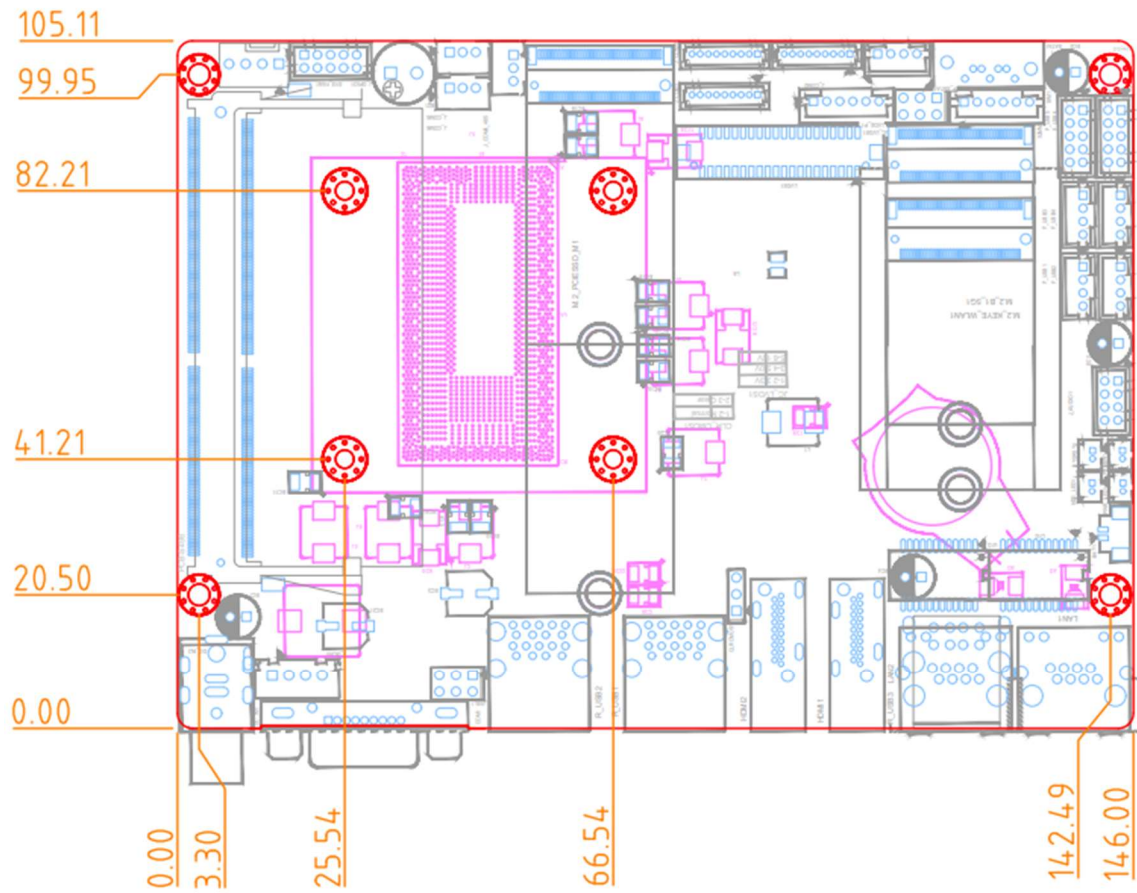
[6]: F\_USB6 only support by Premium U.

[7]: DC\_IN2(DC 12V Power Input Thread Connector) colay with DC\_IN1(DC 12V Power Input  $\Phi$ 2.5mm Jack) on the same position, support DC\_IN2 by default.

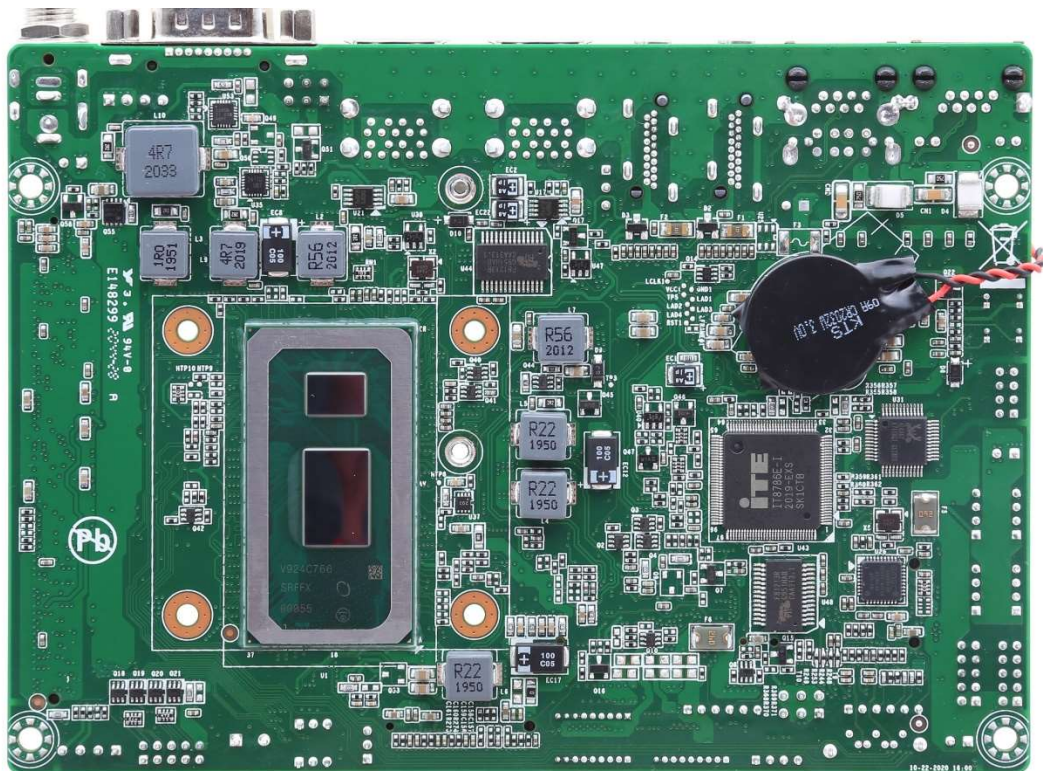
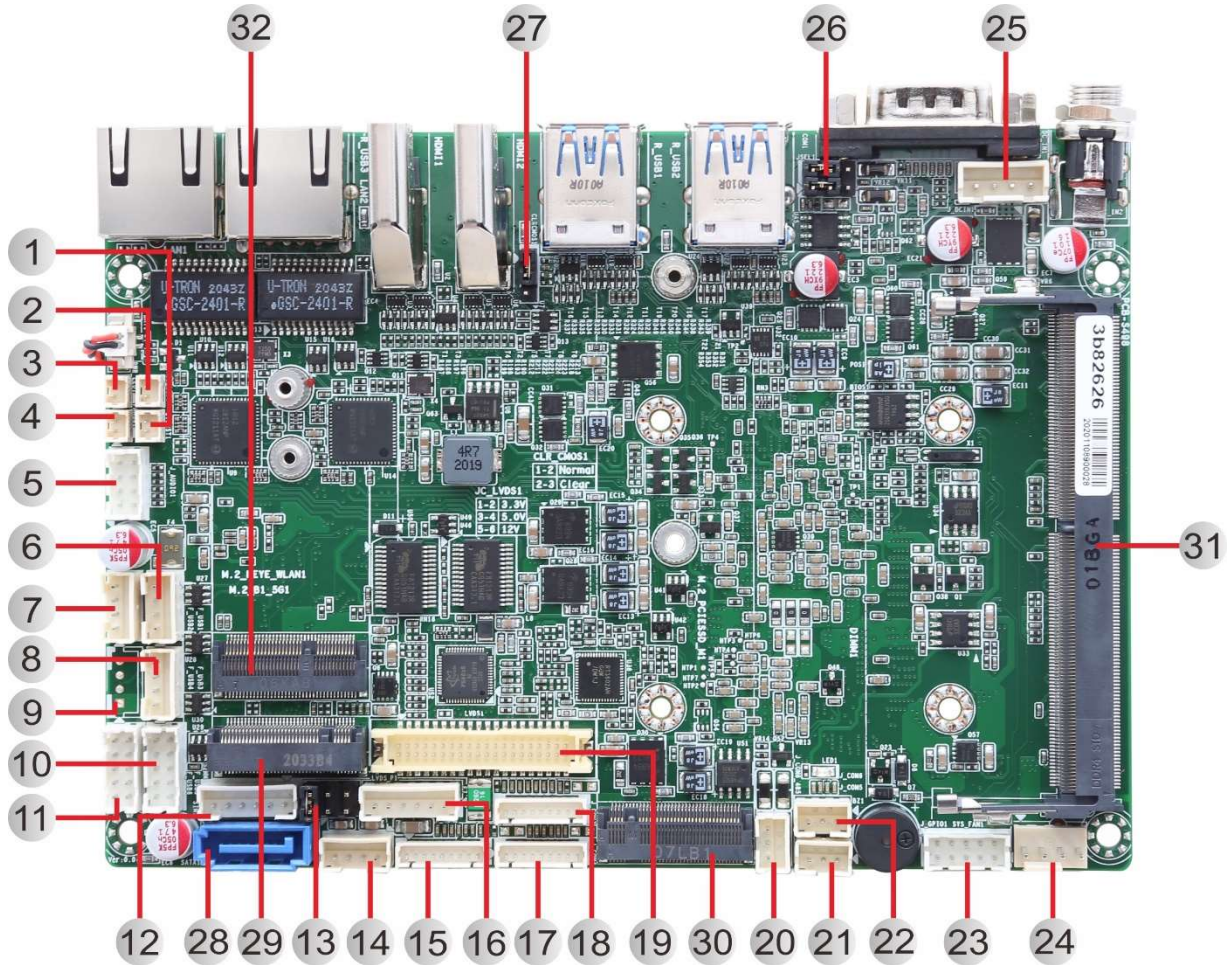
### 3. Functional Block Diagram



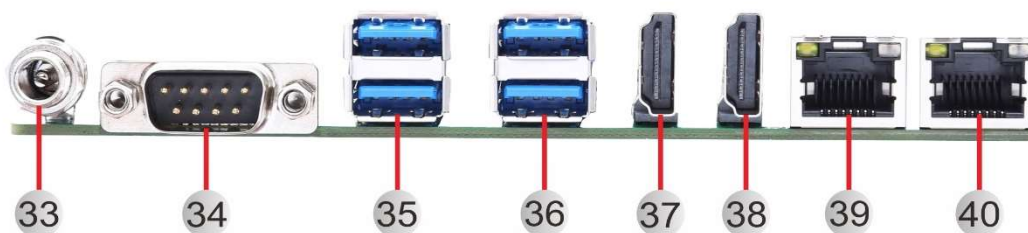
# 4. Mechanical Drawing



## 5. Jumpers / Headers and Connectors








### Jumpers / Headers and Connectors

1	SYSRST1	System Reset Header
2	HDD_LED1	HDD LED Header
3	PWR_LED1	Power LED Header
4	PANSW1	Power Button Header
5	J_AUDIO1	Front Audio Header (Line-Out + MIC)
6	F_USB1	Front USB2.0 Header1
7	F_USB2	Front USB2.0 Header2
8	F_USB3	Front USB2.0 Header3
9	F_USB4	Front USB2.0 Header4 (Colay with M.2_B1_5G1, Default not on board)
10	F_USB5	Front USB2.0 Header5
11	F_USB6	Front USB2.0 Header6 (Only support by Premium-U)
12	SIM1	SIM Card Header
13	JC_LVDS1	eDP/LVDS VDD Select Jumper
14	P_SATA1	SATA Power Header
15	J_COM2	COM2 Header
16	LVDS_P1	eDP/LVDS Backlight Control Header
17	J_COM4	COM4 Header
18	J_COM3	COM3 Header
19	LVDS1	eDP/LVDS Signal Header
20	J_COM6_485	COM6 RS485 Header
21	J_COM5	COM5 Header
22	J_COM6	COM6 RS232 Header
23	J_GPIO1	GPIO Header
24	SYS_FAN1	System FAN Header
25	J_DCIN1	DC 12V Power Input Header
26	JSEL1	COM1 RS232/485 Select Jumper
27	CLRCMOS1	CMOS Clear Jumper
28	SATA1	SATA3.0 7P Connector
29	M.2_B1_5G1	M.2 (NGFF) Key-B Slot (3042/3052, PCIE + USB3.0(Premium-U) + USB2.0, support 4G/5G)
30	M.2_PCIESSD_M1	M.2 (NGFF) Key-M/B Slot (PCIe x4 NVMe/ SATA SSD, 2242/2280) Only SATA for Base-U or NVMe/ SATA Auto detected for Premium-U


31	DIMM1	DDR4 SO-DIMM Slot
32	M.2_KEYE_WLAN1	M.2 (NGFF) Key-E Slot (PCIE+USB2.0, WIFI+BT, 2230)
33	DC_IN2 (DC_IN1)	DC 12V Power Input Thread Connector (DC 12V Power Input $\Phi$ 2.5mm Jack Optional)
34	COM1	COM1 DB9/M Connector
35	R_USB2	Dual USB3.0 TYPE-A Connector2
36	R_USB1	Dual USB3.0 TYPE-A Connector1
37	HDMI2	HDMI Upright TYPE-A Connector2
38	HDMI1	HDMI Upright TYPE-A Connector1
39	LAN2 (R_USB3)	GBE LAN RJ45 Connector2 (Dual USB2.0 TYPE-A Connector Optional)
40	LAN1	GBE LAN RJ45 Connector1

## 6. Definition of Jumpers /Headers and Connectors


### 1) SYSRST1 (System Reset Header 2\*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	RESET+	2	RESET-


### 2) HDD\_LED1 (HDD LED Header 2\*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	HDD 3.3V LED+	2	HDD 3.3V LED-

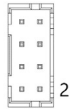
### 3) PWR\_LED1 (Power LED Header 2\*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	POWER 3.3V LED+	2	POWER 3.3V LED-


### 4) PANSW1 (Power Button Header 2\*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	POWER+	2	POWER-

### 5) J\_AUDIO1 (Front Audio Header (Line-Out + MIC) 4\*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	2	LINE_OUT_R	1	MIC_IN_R
	4	GND_AUD	3	GND_AUD
	6	GND_AUD	5	GND_AUD
	8	LINE_OUT_L	7	MIC_IN_L


**6) F\_USB1 (Front USB2.0 Header1 4\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	3	USB2_5+ [1]
	2	USB2_5- [1]	4	GND

**Notes:**

[1]: USB2\_5 Signal of F\_USB1 colay with R\_USB3, default support F\_USB1. (resistor selectable)


**7) F\_USB2 (Front USB2.0 Header2 4\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	3	HUB_USB2_1+ [1]
	2	HUB_USB2_1- [1]	4	GND


**Notes:**

[1]: HUB\_USB2\_1 Signal of F\_USB2 colay with R\_USB3, default support F\_USB2. (resistor selectable)

**8) F\_USB3 (Front USB2.0 Header3 4\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	3	HUB_USB2_4+
	2	HUB_USB2_4-	4	GND

**9) F\_USB4\* (Front USB2.0 Header4 4\*1 Pin 2.00mm)**

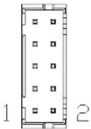
Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	3	USB2_7+ [1]
	2	USB2_7- [1]	4	GND

**Notes:**

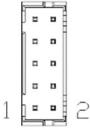
[\*]: F\_USB4 is not on board by default.

[1]: USB2\_7 Signal of F\_USB4 colay with M.2\_B1\_5G1, default support M.2\_B1\_5G1. (resistor selectable)

**10) F\_USB5 (Front USB2.0 Header5 5\*2 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	2	+ 5V	1	+ 5V
	4	HUB_USB2_2-	3	HUB_USB2_3-
	6	HUB_USB2_2+	5	HUB_USB2_3+
	8	GND	7	GND
	10	N/C	9	GND


**11) F\_USB6\* (Front USB2.0 Header6 5\*2 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	2	+ 5V	1	+ 5V
	4	USB2_8-	3	USB2_9-
	6	USB2_8+	5	USB2_9+
	8	GND	7	GND
	10	N/C	9	GND


**Notes:**

[\*]: F\_USB6 only support by Premium U.


**12) SIM1 (SIM Card Header 6\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	UIM_PWR	4	UIM_CLK
	2	GND	5	UIM_RST
	3	UIM_DAT	6	UIM_VPP

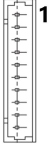
**13) JC\_LVDS1 (eDP/LVDS VDD Select Jumper 3\*2 Pin 2.54 mm)**

Graphic	Setting	Function
	1-2(Default)	+ 3.3V
	3-4	+ 5V
	5-6	+ 12V

**14) P\_SATA1 (SATA Power Header 4\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	+ 12V	3	GND
	2	GND	4	+ 5V

### 15) J\_COM2 (COM2 Header 9\*1 Pin 1.25mm)


Graphic	Pin	Definition	Pin	Definition
	1	COM2_PIN1 [1]	6	COM2_CTS#
	2	COM2_DSR#	7	COM2_DTR#
	3	COM2_RXD	8	COM2_PIN9 [2]
	4	COM2_RTS#	9	GND
	5	COM2_TXD		

**Notes:**

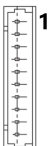
[1]: Pin1 of COM2 is DCD# by default, 5V/12V is available if specified. (resistor selectable)

[2]: Pin9 of COM2 is RI# by default, 5V is available if specified. (resistor selectable)

### 16) LVDS\_P1 (eDP/LVDS Backlight Control Header 6\*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	eDP/LVDS_BKLT_EN
	2	GND	5	+ 12V
	3	eDP/LVDS_BKLT_CTL	6	+ 12V

### 17) J\_COM4 (COM4 Header 9\*1 Pin 1.25mm)

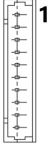
Graphic	Pin	Definition	Pin	Definition
	1	COM4_PIN1 [1]	6	COM4_CTS#
	2	COM4_DSR#	7	COM4_DTR#
	3	COM4_RXD	8	COM4_PIN9 [2]
	4	COM4_RTS#	9	GND
	5	COM4_TXD		

**Notes:**

[1]: Pin1 of COM4 is N/C by default, 5V/12V is available if specified. (resistor selectable)

[2]: Pin9 of COM4 is N/C by default, 5V is available if specified. (resistor selectable)

### 18) J\_COM3 (COM3 Header 9\*1 Pin 1.25mm)

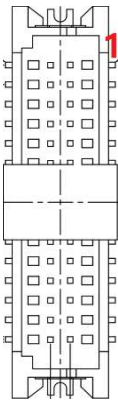
Graphic	Pin	Definition	Pin	Definition
	1	COM3_PIN1 <sup>[1]</sup>	6	COM3_CTS#
	2	COM3_DSR#	7	COM3_DTR#
	3	COM3_RXD	8	COM3_PIN9 <sup>[2]</sup>
	4	COM3_RTS#	9	GND
	5	COM3_TXD		

**Notes:**

[1]: Pin1 of COM3 is DCD# by default, 5V/12V is available if specified. (resistor selectable)

[2]: Pin9 of COM3 is RI# by default, 5V is available if specified. (resistor selectable)

### 19) LVDS1 (eDP/LVDS Signal Header 20\*2 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	2	VDD_PANEL <sup>[1]</sup>	1	VDD_PANEL <sup>[1]</sup>
	4	GND	3	LVDS_PRSENT#/ N/C <sup>[2]</sup>
	6	VDD_PANEL <sup>[1]</sup>	5	VDD_PANEL <sup>[1]</sup>
	8	LVDS_B_DATA0-/ EDP_TX0- <sup>[2]</sup>	7	LVDS_A_DATA0-/ N/C <sup>[2]</sup>
	10	LVDS_B_DATA0+/ EDP_TX0+ <sup>[2]</sup>	9	LVDS_A_DATA0+/ N/C <sup>[2]</sup>
	12	GND	11	GND
	14	LVDS_B_DATA1-/ EDP_TX1- <sup>[2]</sup>	13	LVDS_A_DATA1-/ N/C <sup>[2]</sup>
	16	LVDS_B_DATA1+/ EDP_TX1+ <sup>[2]</sup>	15	LVDS_A_DATA1+/ N/C <sup>[2]</sup>
	18	GND	17	GND
	20	LVDS_B_DATA2-/ EDP_TX2- <sup>[2]</sup>	19	LVDS_A_DATA2-/ N/C <sup>[2]</sup>
	22	LVDS_B_DATA2+/ EDP_TX2+ <sup>[2]</sup>	21	LVDS_A_DATA2+/ N/C <sup>[2]</sup>
	24	GND	23	GND
	26	LVDS_B_CLK-/ EDP_TX3- <sup>[2]</sup>	25	LVDS_A_CLK-/ N/C <sup>[2]</sup>
	28	LVDS_B_CLK+/ EDP_TX3+ <sup>[2]</sup>	27	LVDS_A_CLK+/ N/C <sup>[2]</sup>
	30	GND	29	GND
	32	N/C / EDP_HPDP# <sup>[2]</sup>	31	N/C


34	GND	33	GND
36	LVDS_B_DATA3-/ EDP_AUX- [2]	35	LVDS_A_DATA3-/ N/C [2]
38	LVDS_B_DATA3+/ EDP_AUX+ [2]	37	LVDS_A_DATA3+/ N/C [2]
40	GND	39	N/C

**Notes:**

[1]: Panel Power VDD is 3.3V by default, 5V/12V is selectable by “eDP/LVDS VDD Select Jumper” (JC\_LVDS1, Table 13).

[2]: It supports LVDS by default and can supports eDP if specified. (resistor selectable)


**20) J\_COM6\_485\* (COM6 RS485 Header 3\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	COM6_RS485+	3	GND
	2	COM6_RS485-		


**Notes:**

[\*]: J\_COM6\_485 and J\_COM6 can be on the board at the same time, but they can't be accessed simultaneously.

**21) J\_COM5 (COM5 Header 3\*1 Pin 2.00mm)**

Graphic	Pin	Definition	Pin	Definition
	1	COM5_RXD	3	GND
	2	COM5_TXD		

**22) J\_COM6\* (COM6 RS232 Header 3\*1 Pin 2.00mm)**

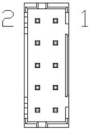
Graphic	Pin	Definition	Pin	Definition
	1	COM6_RXD	3	GND
	2	COM6_TXD		

**Notes:**

[\*]: J\_COM6\_485 and J\_COM6 can be on the board at the same time, but they can't be accessed simultaneously.



**23) J\_GPIO1 (GPIO Header 5\*2 Pin 2.00mm)**


Graphic	Pin	Definition	Pin	Definition
	2	SIO_GPI70 (0xA06 Bit0, H <sup>[1]</sup> )	1	SIO_GPI71 (0xA06 Bit1, H)
	4	SIO_GPI72 (0xA06 Bit2, H)	3	SIO_GPI73 (0xA06 Bit3, H)
	6	SIO_GPO74 (0xA06 Bit4, H)	5	SIO_GPO75 (0xA06 Bit5, H)
	8	SIO_GPO76 (0xA06 Bit6, H)	7	SIO_GPO77 (0xA06 Bit7, H)
	10	+ 3.3V <sup>[2]</sup>	9	GND

**Notes:**


[1]: "H" or "L" means the default voltage is High or Low level. (3.3V GPIO)

[2]: Power on this Pin is 3.3V by default, 5V is available if specified. (resistor selectable)


**24) SYS\_FAN1 (System FAN Header 4\*1 Pin 2.54mm)**

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	+ 12V	4	FAN Speed Control


**25) J\_DCIN1 (DC 12V Power Input Header 4\*1 Pin 2.54mm)**

Graphic	Pin	Definition	Pin	Definition
	1	+ 12V_IN	3	GND
	2	+ 12V_IN	4	GND

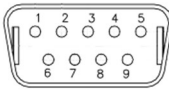
**26) JSEL1 (COM1 RS232/485 Select Jumper 3\*2 Pin 2.54 mm)**

Graphic	Setting	Function
	1-3, 2-4(Default)	RS232 (COM1_PIN1: DCD COM1_PIN2: RXD)
	3-5, 4-6	RS485 (COM1_PIN1: RS485- COM1_PIN2: RS485+)

### 27) CLRCMOS1 (CMOS Clear Jumper 3\*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Clear CMOS

### 34) COM1 (COM1 DB9/M Connector)

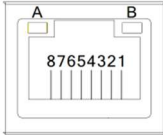
Graphic	Pin	Definition	Pin	Definition
	1	COM1_PIN1 [1]	6	COM1_DSR#
	2	COM1_PIN2 [1]	7	COM1_RTS#
	3	COM1_TXD	8	COM1_CTS#
	4	COM1_DTR#	9	COM1_PIN9 [2]
	5	GND		

**Notes:**

[1]: COM1 can be RS232 / RS485 by selecting JSEL1 Jumper, check Table26 for detail. When COM1 support RS232, Pin1 of COM1 is DCD# by default, 5V/12V is available if specified. (resistor selectable)

[2]: Pin9 of COM1 is RI# by default, 5V is available if specified. (resistor selectable)

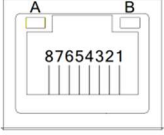
### 39) LAN2\* (GBE LAN RJ45 Connector2 8Pin)

Graphic	Pin	Definition	Pin	Definition	
	1	MDI0_2+	5	MDI2_2-	
	2	MDI0_2-	6	MDI1_2-	
	3	MDI1_2+	7	MDI3_2+	
	4	MDI2_2+	8	MDI3_2-	
	A	Active LED	ACT: Twinkling Yellow Only LINK: Lights On Stop: Lights Off	B	Speed LED

**Notes:**

[\*]: LAN2 colay with R\_USB3, default support LAN2.

**40) LAN1 (GBE LAN RJ45 Connector1 8Pin)**

Graphic	Pin	Definition	Pin	Definition	
	1	MDI0_1+	5	MDI2_1-	
	2	MDI0_1-	6	MDI1_1-	
	3	MDI1_1+	7	MDI3_1+	
	4	MDI2_1+	8	MDI3_1-	
	A	Active LED	ACT: Twinkling Yellow	B	Speed LED
		Only LINK: Lights On	100M: Turn Green		
		Stop: Lights Off	10M: Lights Off		

## 7. BIOS setup

See “BIOS Spec for SYS8F400VGGA-8265U Series” for detail information of BIOS setup.

**【End】**